DEMOCRITUS UNIVERSITY OF THRACE
SPACE RESEARCH LABORATORY

DUTH/SRL- Document Designation:

DUTH/SRL-pSIF-Data Sheet

pSIF-ASIC

Preliminary Data Sheet

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Revision History

Revision	Release Date	Comments
Ver.1	1/8/2007	Original version
Ver.2	12/10/2007	Updated version

Table of Contents

1 Introduction

This document describes the main functionalities along with the main characteristics of the pSIF device. As the design advances into phase 3, this document will be further enhanced. It will be finalized after the validation phase of the FM design.

2 Functionality

pSIF is a rad-hard, mixed signal analog digital device developed by DUTH/SRL designed to interface up to 4 pressure sensors. The main functionalities of the pSIF device are listed below

- Bias the sensor either with a constant voltage or a constant current.
- Convert to a digital value the differential sensor as well as the bias voltage.
- Transmit the quantized sensor data to the S/C through the I2C bus.

3 Key Features

- Up to 4 pressure sensors can be biased and quantized by the ASIC.
- 14 bit ADC converter
- Built in Voltage reference
- Instrumentation amplifier for small differential signal measurements
- Adjustable gain for various pressure range measurements
- Precision current source used for sensor temperature compensation. Can also be used for temperature measurements.
- I2C Protocol interface

- Single power supply (3.3 or 2.5V) (Internal voltage regulator)
- Low power (<10mW/25mW including sensor current.)
- Autonomous operation on power up
- Wide Temperature Operating range (-55 to 125 deg C)
- Radhard up to 1 Mrad
- SEL free up to 120 MeV/mg/cm^2
- Immune to SEU up to a LET threshold of 120 MeV/mg/cm^2
- Available as bare die.

4 Applications

- Digital Pressure Sensors
- Temperature measurement.
- Housekeeping in space instrumentation

5 Block Diagram

The block diagram of the pSIF ASIC is shown in Fig. 1. .

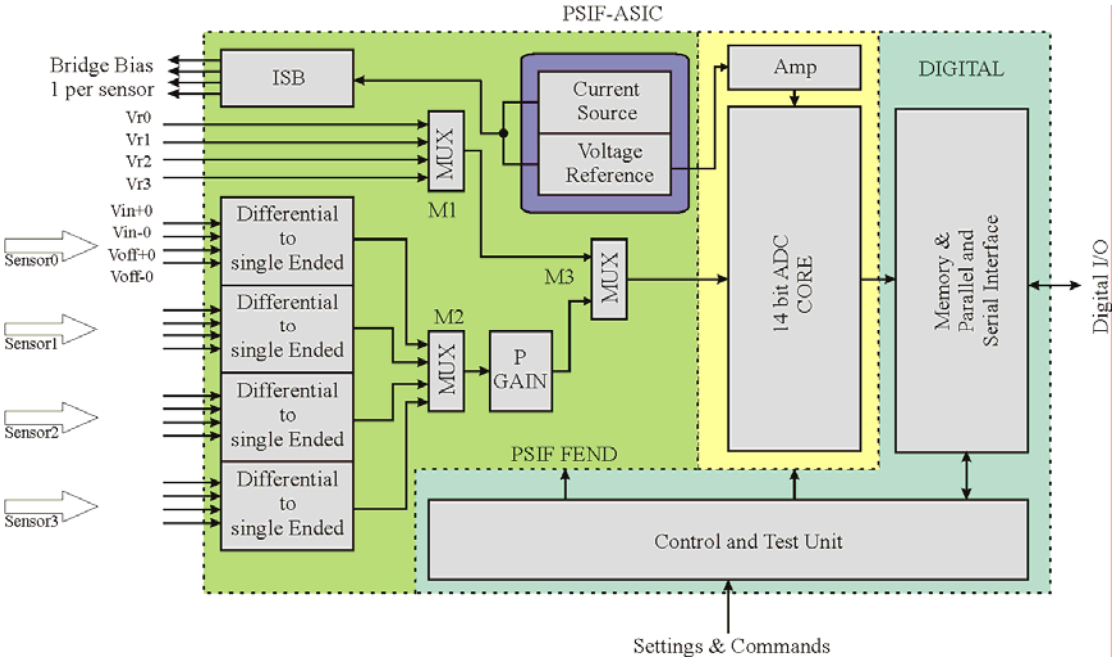

Fig. 1. Overall block diagram of the pSIF ASIC.

It consists of

- ISB Circuit that handles the biasing of the sensors attached to the device
- 4 Differential to Single Ended Conversion Unit (one per sensor). The DSE stages apart from converting the differential voltage to a single ended, they also provide a gain of 40dB.
- An programmable amplification unit (pgain). The gain of this unit is programmed through an I2C command.
- 3 Multiplexers that direct the input voltages to the ADC core
- A Current Source that is used for providing a bias current to the sensor.
- A Voltage Reference that is used to provide a constant voltage to the sensors as well as to the ADC core.
- An ADC core
- A Memory together wit a parallel and serial interface unit.
- A Control and Test Unit

6 Sensor Interface Setup

The pressure sensor-pSIF ASIC interface is shown in Fig. 2. Only one sensor (out of the 4 that can be attached) is shown for simplicity reasons. Pad BS is used to bias the sensor. Pad VR is the single ended voltage that is converted directly through the ADC and is used for temperature compensation of the sensor. Pads Vin+ and Vin- are connected directly to the sensor. It is through these pads that the differential bridge voltage is fed into the pSIF ASIC. Pads Voff+ and Voff- are used to add/subtract an offset voltage to the differential bridge voltage (Requirement by Presens). The offset voltage can be set through external resistors R1-R3 as shown in Fig. 3.

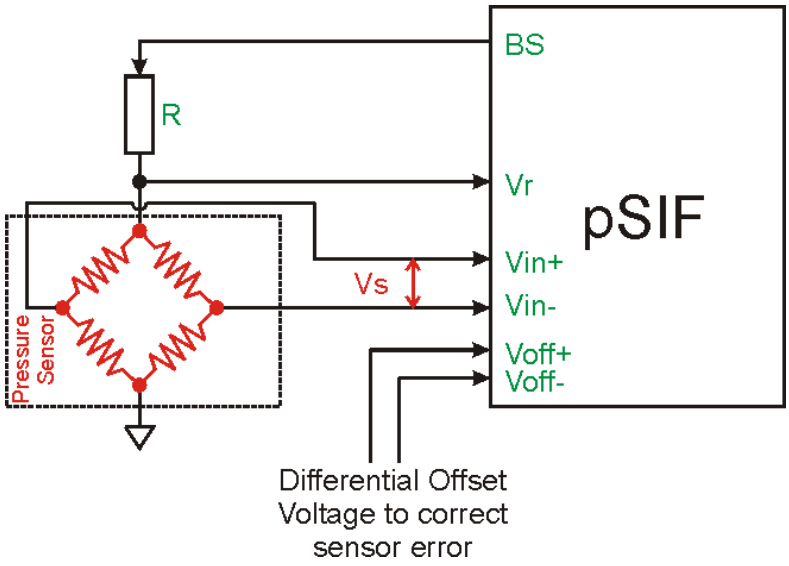

Fig. 2. Block diagram of the sensor connection to the pSIF.

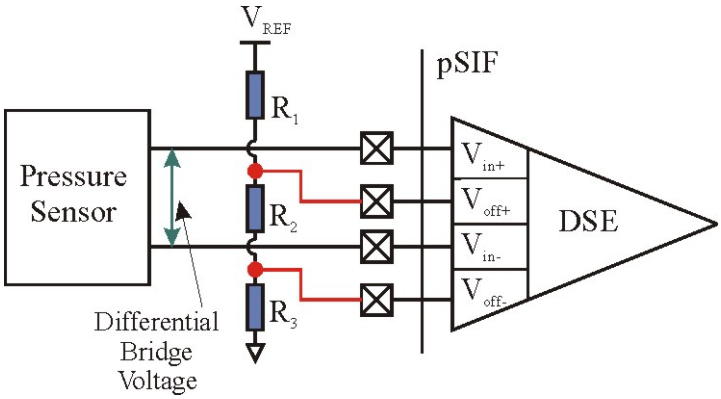

Fig. 3. Generation of Voff+ and Voff-.

The values of R1, R2 and R3 are defined per chip and per sensor

7 Sensor Quantization

pSIF initially quantizes the differential bridge voltage Vs which is proportional to the applied pressure and ten Vr which is used for temperature compensation of the sensor.

8 pSIF fix scan Configurations

pSIF device has two modes of measurement regarding the 4 sensors that it interfaces. In the **scan** mode the device quantizes each sensor sequentially. In the **fix** mode it performs ADC conversions only on one sensor. The sensor that is interfaced is programmed by a command. The command can be issued by either the serial or the parallel interface.

9 Sensor Biasing and Inactive Sensor Configuration

pSIF can bias the pressure sensor either with a constant voltage or a constant current. The selection is performed through a command issued from the I2C bus.

During the time that a specific sensor is interfaced, the other three connected sensors to the pSIF device (inactive sensors) are kept in a biased state through the inactive sensor bias (ISB) subsystem of the ASIC. The ISB circuit has the ability to be de-activated. The biasing of the inactive sensors is essential to guarantee a good performance. The sensor biasing network is shown in Fig. 4

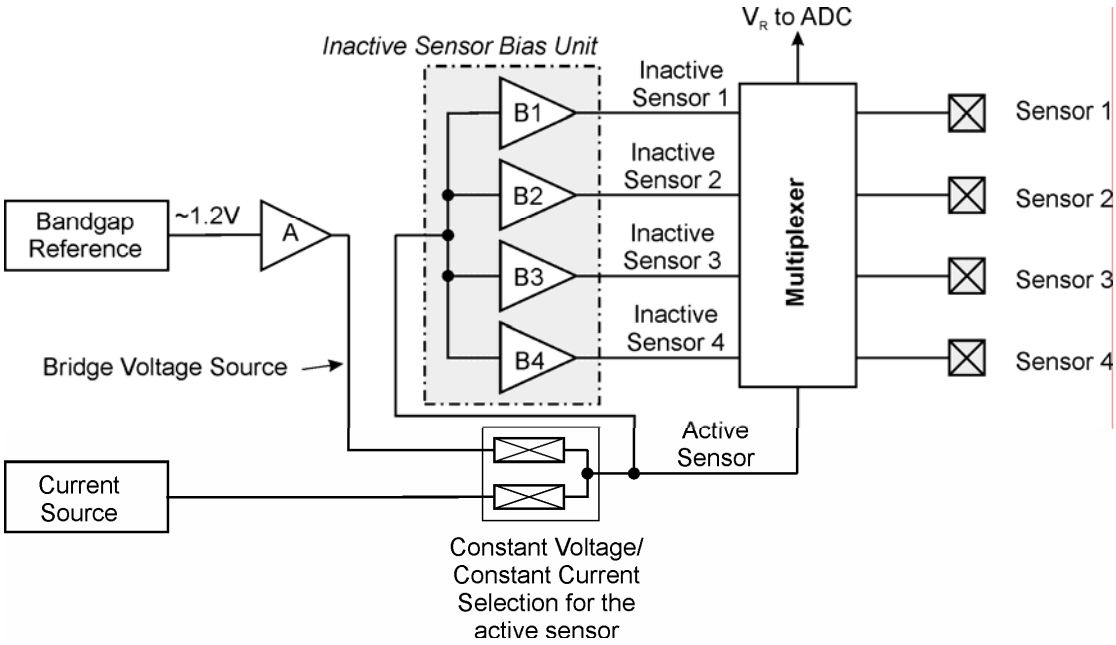

Fig. 4. Sensor biasing block diagram of the pSIF ASIC.

A copy of the developed voltage (no matter if it is biased on constant voltage or constant current) on the active sensor is copied to the inactive ones through buffers B1-B4.

10 Gain Selection

4 gain values are provisioned in the pSIF device for the differential bridge voltage Vs: 100, 800, 6400, 10000. The user can select any of these configurations depending on the full scale pressure that needs to be measured and the pressure sensor used. The selection is done through the I2C interface.

11 Digital Interface

pSIF has two digital interfaces.

- A parallel interface
- A serial I2C interface

The selection of the active interface is performed through pad PAR_I2Cb. Logic low selects the I2C interface. Logic high selects the parallel interface.

11.1 The Parallel Interface

The parallel interface is mostly used for testing purposes. Many pSIF devices can be connected on the same bus. The parallel interface consists of the following pads/buses:

- A data bus (DB[13..0])
- An address bus (AB[7..0])
- Pad Csb_par. Used to select the current chip.
- Pad Rwb_par Used to select between read and write mode.

11.2 The I2C interface

The I2C protocol is the main digital serial interface unit in typical applications. It is used for sensor data read-out and for commanding the device.

The I2C bus housing one master and many pSIF devices is shown in Fig. 5.

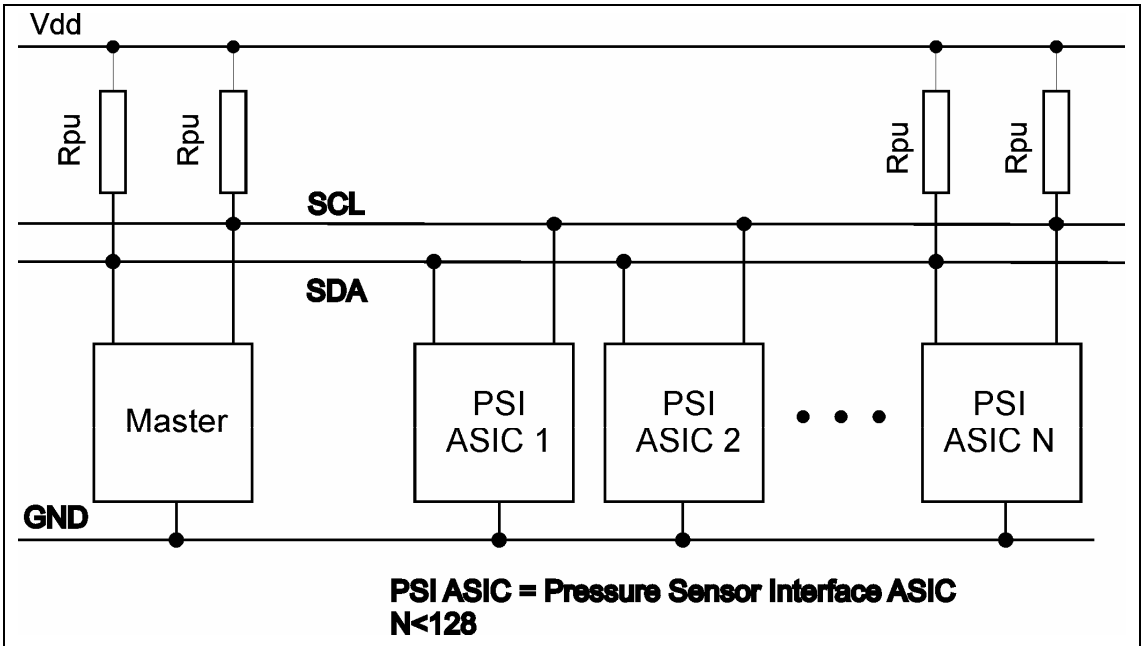

Fig. 5. I2C bus configuration.

The bus consists of two lines

- The serial data bus (SDA) line
- The serial clock (SCL) line

The SDA line can be controlled both by the master (external microcontroller) and by any pSIF device that is transmitting. The SCL line is controlled only by the master. Up to 128 pSIF devices can be connected to the bus. Each device will have a unique serial address set by hard pins on the board level.

Both SCL and SDA lines can be operated anywhere between 2.5 and 3.3V. The pull up resistor fro the SDA line can be in the range from 120 Ohms to 10K.

For more information on the I2C interface and the relative commands the user should read “DUTH-SRL-pSIF-users-mannual”.

12 Use of pSIF for voltage and temperature monitoring applications

12.1 Voltage monitoring Applications.

12.1.1 Single Ended Voltage Monitoring Applications

pSIF can be used for voltage monitoring purposes in a S/C. In both cases the user can de-activate (bias off) the DSE and ISB stages as well as the current source. In such applications the user applies a voltage on pads VRx (x=0-3) which is directly quantized by the ADC. Up to 4 discrete voltages can be monitored in thi configuration.

12.1.2 Differential Voltage Monitoring Applications

pSIF can be used for differential voltage monitoring applications. In this scenario the user has to apply the differential voltage to the DSE stage. Offset addition can be canceled by placing both Voff+ and Voff- to ground. The DSE can operate at common modes ranging from 0.3 to 1.9V. Up to 4 differential voltages can be monitored in this configuration.

12.2 Temperature Monitoring Applications

In addition, pSIF can be used for temperature monitoring applications using PRT and NTC sensors. In this case the PRT/NTC sensor is attached to VRx pads. The current source is used to provide a constant (temperature independent) current to the sensors. The voltage developed on the sensor (which is directly proportional to the sensors temperature) is quantized by the ADC. Up to 4 temperatures can be measured in this configuration. It is noted that the current source must be activated in this configuration.

12.3 Mixed mode applications

It is possible to use the device in a mixed mode application where 4 differential voltages and 4 temperature/or single ended voltages are monitored.

13 Extension of the sample channels by use of an external multiplexer.

It is possible to extend the number of channels that can be attached to the pSIF device by using an external multiplexer.

14 Analog Sampling Electrical Characteristics

- Full scale Reference voltage 0 -2.5 5Vpp
- INL ±0.5 LSB nominal/ ±1 LSB after 1Mrad
- Input Resistance on the analog inputs > 1000Mohm
- Common mode range for the DSE stage: 0.4 to 1.9V

15 Power Supply

pSIF can be powered with a single power supply 3.3V. It utilizes an internal power supply regulator that produces the 2.5 V required by the pSIF core. Alternatively, pSIF can be powered with a single 2.5V power supply. However, in this case the I/O bused will have to be operated at 2.5V.

16 Temperature Characteristics

pSIF device can operate without performance degradation from -55 to 125 deg C.

17 Power Consumption

The power consumption of the pSIF device is less than 25mW (worst case-4 sensors attached to the device and ISB unit on) including the sensor current. The power consumption of the pSIF ASIC itself is less than 10mW and can be as low as 5mW depending on the number of the subsystems activated.

18 Radiation Hardness

18.1 Total Ionizing Dose

pSIF is rad-hard to a TID level above 1 Mrad (Si).

18.2 Single Event Effects

pSIF is immune to SEUs up to an LET threshold of 120 MeV/mg/cm^2 .

No latch up occurs up to an LET threshold of 120 MeV/mg/cm^2 .

19 Packaging Information

pSIF is available as

- 120 CQFP Package./Metal lid/
- Bare die